

Thin Film On Wafer & Substrate

Al - B	C - In	Si - T	S - Z
Aluminum Film on Silicon wafer	CeO ₂ Epi-thin film on YSZ Alloy	Si+SiO ₂ +Pt (Polycrystalline)Thin Film	SiC Film (3C) on Si wafer
AlN Thin Film on Silicon & Sapphire	Diamond on Silicon wafer	Si+SiO ₂ +Ti(or TiO ₂)+Pt Thin Film on Si Wafer	Thermal Oxide Wafer
Au coated Silicon wafer /Microscope Slides	GaN Template on Sapphire& Silicon	SiO ₂ +Si ₃ N ₄ on Silicon wafer	YBCO Epi Film on SrTiO ₃ , LaAlO ₃
Au(single crystal)/Cr coated SiO ₂ /Si substrate	Graphene film on Ni/SiO ₂ /Si	SOS (silicon on Sapphire)	ZnO thin film on Sapphire
AlGaN Template on Sapphire	Graphene Oxide Thin Film on Glass	SOI Wafer (Silicon On Insulator)	
Boron-Nitride on Silicon	InGaAs EPI on InP (Semi-insulating)	Silicon-Nitride on Silicon	

1. AlN Thin Film on Silicon & Sapphire

A. AlN Thin Film on Sapphire

No.	Item	Description
1.	AlN Epitaxial Template on Sapphire (Epi-Film on Sapphire, undoped) 10mmx10mmx1000nm	<p>AlN Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Sizes : 10mmx10mm Substrate Sapphire Orientation: c axis (0001) +/- 1.0 deg. Type and Doping: Undoped, Semi-insulating Macro Defect Density: <5 cm⁻² Front Surface Finish (Al Face): As-grown, Epi-ready Back Surface Finish Sapphire: as-received finish Useable Surface Area: >90% Edge Exclusion Area: 1mm Package: Single Wafer Container AlN layer thickness: 1000 nm
2.	AlN Epitaxial Template on Sapphire (Epi-Film on Sapphire, undoped) 2"x1000nm t- two sides polished	<p>AlN Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Sizes: 2" round Substrate Sapphire Orientation: c axis (0001) +/- 0.5 deg. Type and Doping: Undoped, Macro Defect Density: <5 cm⁻² Front Surface Finish (Al Face): As-grown, Epi-ready Back Surface Finish Sapphire: as-received finish Useable Surface Area: >90% Edge Exclusion Area: 1mm Package: Single Wafer Container AlN layer thickness: 1000 nm Polish: Both sides polished

3.	AlN Epitaxial Template on Sapphire (Epi-Film on Sapphire, undoped) 2"x1000nm t,one side polished	<p>AlN Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Sizes: 2" round • AlN thin film orientation: (0001) • Substrate Sapphire Orientation: c axis (0001) +/- 1.0 deg. • Type and Doping: Undoped, • Macro Defect Density: <5 cm⁻² • Front Surface Finish (Al Face): As-grown, Epi-ready • Back Surface Finish Sapphire: as-received finish • Useable Surface Area: >90% • Edge Exclusion Area: 1mm • Package: Single Wafer Container • AlN layer thickness: 1000 nm • Polish: One side polished
4.	AlN Epitaxial Template on Sapphire (Epi-Thim on Sapphire, undoped) 2"x 5000 nm	<p>AlN Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Sizes: 2" Round • Dimensions: 50mm +/- 2mm • Substrate Sapphire Orientation: c-axis (0001) +/- 1.0deg. • Type and Doping: Undoped, Semi-insulating • Macro Defect Density: <5 cm⁻² • Front Surface Finish (Al Face): As-grown, Epi-ready • Back Surface Finish Sapphire: as-received finish • Useable Surface Area: >90% • Edge Exclusion Area: 1mm • Package: Single Wafer Container • AlN layer thickness: 5000 nm , (± 10%)
5.	AlN Epitaxial Template on Sapphire (Epi-film on Sapphire, undoped) 4"x 5000 nm	<p>AlN Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Sizes: 4" Round • Dimensions: 100 mm +/-2mm • Substrate Sapphire Orientation: c-axis (00.1) +/- 0.3deg. • Type and Doping: Undoped, Semi-insulating • Macro Defect Density: <5 cm⁻² • Front Surface Finish (Al Face): As-grown, Epi-ready • Back Surface Finish Sapphire: as-received finish • Useable Surface Area: >90% • Edge Exclusion Area: 1mm • Package: Single Wafer Container • AlN layer thickness: 5000 nm , (± 10%)
6.	AlN Epitaxial Template on Sapphire (Epi-film on Sapphire, undoped) 4"x 1000 nm	<p>AlN Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Sizes: 4" Round • Dimensions: 100 mm +/- 2mm

	<ul style="list-style-type: none"> • Substrate Sapphire Orientation: c-axis (00.1) +/- 0.3deg. • Type and Doping: Undoped, Semi-insulating • Macro Defect Density: <5 cm⁻² • Front Surface Finish (Al Face): As-grown, Epi-ready • Back Surface Finish Sapphire: as-received finish • Useable Surface Area: >90% • Edge Exclusion Area: 1mm • Package: Single Wafer Container • AlN layer thickness: 1000 nm , (iÀ 10%)
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B. AlN Thin Film on Silicon

No.	Item	Description
1.	AlN Epitaxial Template on Silicon (Epi-film on <111> Si, undoped N type) 10mmx10mm x 200 nm	<p>AlN Epitaxial Template on Silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template on Silicon is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Nominal AlN thickness: 200nm ±10%, one side coated • Front Surface: <1nm RMS, as-grown • Back surface: silicon as received • AlN orientation: (00.2) • Macro Defect Density: <1/cm² • Wafer base: Silicon [111] 10x10 x0.5 mm, one side polished
2.	AlN Epitaxial Template on 2" Silicon (Epi-film on <111> Si, undoped N type) 2"x 200 nm	<p>AlN Epitaxial Template on Silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template on Silicon is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Nominal AlN thickness: 200nm ±10%, one side coated • Front Surface: <1nm RMS, as-grown • Back surface: silicon as received • AlN orientation: (00.2) • Macro Defect Density: <1/cm² • Wafer base: Silicon [111] N type, 2" dia x0.5 mm, res: 1~10 ohm-cm, one side polished
3.	AlN Epitaxial Template on 4" Silicon (Epi-film on <111> Si, undoped N type) 4"x 200 nm	<p>AlN Epitaxial Template on Silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. Epi AlN template on Silicon is a cost effective way to replace AlN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Nominal AlN thickness: 200nm ±10%, one side coated • Front Surface: <1nm RMS, as-grown • Back surface: silicon as received • AlN orientation: (00.2) • Macro Defect Density: <1/cm² • Wafer base: Silicon [111] N type, 4" dia x0.5 mm, res: 1~10 ohm-cm, one side polished

2. Au coated Silicon wafer /Microscope Slides

No.	Item	Description
1.	Au(Gold) Coated Microscope Slides,Gold layer thickness: 50nm (+/- 5nm),Glass slide: 75 x 25mm	<p>High quality glass, standard microscope slides coated with 50nm of gold with a 5nm chromium adhesion layer between the glass slide surface and the gold coating. Can be used for a wide range of nanotechnology, biotechnology and AFM applications and is also suitable of an opaque microscopy support. Both Cr and Au are evaporated on the glass slide using a vacuum evaporation system. The gold surface is not atomically flat, but has bumps in the nm range. The gold slides are individually packed in a slide mailer. The gold slides are autoclavable.</p> <p><u>Specifications:</u> Glass slide: 75 x 25mm , 1mm thickness, soda lime glass Chromium adhesion layer thickness: 5nm Gold layer thickness: 50nm (+/- 5nm)</p>
2.	Au(Gold) coated on Si(111) substrate(P-type B-doped,) ,4"x0.5 mm,1sp Au= 50nm (\pm 5nm)	<p>4" gold coated silicon wafers, useful for a variety of applications such as SEM or AFM supports, nanotechnology and biotechnology. Both Cr and Au are evaporated on the silicon wafers using a vacuum evaporation system with chromium between the glass and the gold to serve as an adhesion layer. The gold surface is not atomically flat, but has bumps in the nm range. The wafers are packed and shipped in a wafer carrier. Au coating should be stable to about 175° C; above that temperature delamination could occur.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Film: Au coated on Si substrate ,4"x0.5 mm,1sp P-type B-doped, <ul style="list-style-type: none"> ▪ Au=50nm (\pm 5nm) ▪ Si(100) P type B doped ~500 um Prime Grade • Resistivity: N/A • Substrate Size: 4" diameter +/- 0.5 mm x 0.5 mm • Polish: one side polished • Surface roughness: < 5A • Optional: you may need tool below to handle the wafer (click picture to order)

3. AlGaN Template on Sapphire

No.	Item	Description
1.	Al(0.1)Ga(0.9)N Epitaxial Template on Sapphire (C plane), N type, undoped, 2"x 5 micron,1sp,Research Grade	<p>Al(0.1)Ga(0.9)N Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template is a cost effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Sizes 2" Round • Dimensions 50.8mm +/- 0.25mm • Substrate Sapphire, Orientation c-axis (0001) +/- 1.0 o • Conduction Type: n-type, • Resistivity < 0.5 Ohm-cm • Front Surface Finish (Ga Face) As-grown • Back Surface Finish Sapphire as-received finish • Useable Surface Area >90% • Edge Exclusion Area 1mm • Package Single Wafer Container

2.	Al(0.9)Ga(0.1)N Epitaxial Template on Sapphire (C plane), N type, undoped, 2"x 5 micron, 1sp, Research Grade	<p>Al(0.9)Ga(0.1)N Epitaxial Template on sapphire is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template is a cost effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Sizes 2" Round • Dimensions 50.8mm +/- 0.25mm • Substrate Sapphire, Orientation c-axis (0001) +/- 1.0 o • Conduction Type: n-type, • Resistivity < 0.5 Ohm-cm • Front Surface Finish (Ga Face) As-grown • Back Surface Finish Sapphire as-received finish • Useable Surface Area >90% • Edge Exclusion Area 1mm • Package Single Wafer Container
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4. Aluminum on Silicon Wafer

No.	Item	Description
1.	Aluminum Film on Silicon Wafer , 3 microns / 4" -- Al-Si-100-3um ,Si(100) N-type R:<0.005 ohm.cm	<p><u>Aluminum Metallic Film:</u></p> <ul style="list-style-type: none"> • Film coated by E-beam evaporation under vacuum below 10-6 torr • Aluminum Thickness: 3 microns • evaporation rate: 0.2 nanometer per second <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: Si n- type • Resistivity: <0.005 ohm-cm • Size: 4" diameter +/- 0.5 mm x 0.525 +/- 0.025 mm th • Orientation: (100) +/- 0.5o • Polish: One sides polished • Surface roughness: Prime • Packing: Vacuum packed on a 4" single wafer carrier
2.	Aluminum Film on Silicon Wafer , 3 microns / 4" -- Al-Si-100-3um ,Si(100) N-type R:1-10 ohm.cm	<p><u>Aluminum Metallic Film:</u></p> <ul style="list-style-type: none"> • Film coated by E-beam evaporation under vacuum below 10-6 torr • Aluminum Thickness: 3 microns • evaporation rate: 0.2 nanometer per second <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: Si n- type • Resistivity: 1- 10 ohm-cm • Size: 4" diameter +/- 0.5 mm x 0.525 +/- 0.025 mm th • Orientation: (100) +/- 0.5o • Polish: One sides polished • Surface roughness: Prime • Packing: Vacuum packed on a 4" single wafer carrier

5. Au (epi) /Cr coated SiO₂/Si substrate

No.	Item	Description
1.	Au (highly oriented polycrystalline) /Cr coated SiO ₂ /Si substrate , 6"x0.675 mm,1sp P-type B-doped, Au(111)=150 nm, Cr=20nm	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Film: Au/Cr coated SiO₂/Si substrate ,6"x0.675 mm,1sp P-type B-doped, <ul style="list-style-type: none"> Au(111)=150 nm Cr=20nm SiO₂=200 nm Si(100) P type B doped ~675 um Prime Grade Resistivity: <0.005 ohm.cm Substrate Size: 6" diameter +/- 0.5 mm x 0.675 mm Polish: one side polished Surface roughness: < 5A
2.	Au(highly oriented polycrystalline)/Cr coated SiO ₂ /Si substrate ,4"x0.525 mm,1sp P-type B-doped, Au(111)=150 nm, Cr=20nm	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Film: Au/Cr coated SiO₂/Si substrate ,4"x0.525 mm,1sp P-type B-doped, <ul style="list-style-type: none"> Au(111)=150 nm Cr=20nm SiO₂=300 nm Si(100) P type B doped ~525 um Prime Grade Resistivity: <0.005 ohm.cm Substrate Size: 4" diameter +/- 0.5 mm x 0.5 mm Polish: one side polished Surface roughness: < 5A

6. Boron Nitride Film on Silicon Wafer

No.	Item	Description
1.	Boron Nitride Film on Silicon Wafer , 14 microns / 4" -- BN-Si-100-14u	<p><u>Boron Nitride Film:</u></p> <p>Boron nitride is a chemical compound with chemical formula BN, consisting of equal numbers of boron and nitrogen atoms. BN is isoelectronic to a similarly structured carbon lattice and thus exists in various crystalline forms. The Cubic (sphalerite structure) variety analogous to diamond is called c-BN. Its hardness is inferior only to diamond, but its thermal and chemical stability is superior. Low-pressure deposition of thin films of cubic boron nitride are grown on Si (100) wafers for this product.</p> <ul style="list-style-type: none"> BN Film coated by sputtering method BN Thickness: 14 microns +/- 10% <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: Si n- type Resistivity: 1- 10 ohm-cm Size: 4" diameter +/- 0.5 mm x 0.525 +/- 0.025 mmth Orientation: (100) +/- 0.5o Polish: One sides polished Surface roughness: Prime Packing: Vacuum packed on a 4" single wafer carrier box

7. CeO₂ Epi-thin film on YSZ Alloy

No.	Item	Description
1.	CeO ₂ Epi Film (40 nm one side) on YSZ <100> 10x10x0.5 mm.	<u>Main Specifications</u> Epitaxial thin Film Composition: <100> CeO ₂ Epitaxial Film Thickness: 40 nm +/- 10 nm Epitaxial FWHM: < 5 o Substrate: <100>, YSZ, 10x10x0.5 mm, one side polished Package Sealed in Vacuum in a plastic box and bag.
2.	CeO ₂ Epi Film (40 nm one side) on YSZ, <111>10x10x0.5 mm, 1sp	<u>Main Specifications:</u> Epitaxial thin Film Composition: <111> CeO ₂ Epitaxial Film Thickness: 40 nm +/- 10 nm Epitaxial FWHM: < 5 o +/- 1o Substrate: <111>, YSZ, 10x10x0.5 mm, one side polished Package Sealed in Vacuum in a plastic box and bag.

8. Diamond on Silicon wafer

No.	Item	Description
1.	Diamond on Oxide (DOI) Wafer, 4" , 2 um Thick, 10 nm Ra	<u>Specifications:</u> <ul style="list-style-type: none"> • Wafer Size: 4" diameter x 0.5mm • Si wafer Orientation: (100) +/- 0.5o • Insulating Layer: SiO₂ • Diamond film thickness: 2 microns,, Oxide Layer: 1 micron • Resistivity: 10E3 ~ 10E4 ohm-cm • Surface Roughness: as grown , RA < 10 nm • Package: One 1000 class clean room with 100 class plastic bag
2.	Diamond on Silicon Wafer, 4" , 2 um Thick, 10 nm Ra	<u>Specifications:</u> <ul style="list-style-type: none"> • Wafer Size: 4" diameter x 0.5mm • Si wafer Orientation: (100) +/- 0.5o • Diamond film thickness: 2 micron • Resistivity: 10E3 ~ 10E4 ohm-cm • Surface Roughness: as grown , RA < 10 nm • Package: One 1000 class clean room with 100 class plastic bag
3.	Electric Conductive Diamond on Insulator Wafer, 4" , 2 um Thick, 10 nm Ra	<u>Specifications:</u> <ul style="list-style-type: none"> • Wafer Size: 4" diameter x 0.5mm • Si wafer Orientation: (100) +/- 0.5o • Insulating Layer: SiO₂ • Diamond film thickness: 2 micron,, Oxide Layer: 1 micron • Resistivity: <0.1 ohm-cm • Surface Roughness: as grown , RA < 10 nm • Package: One 1000 class clean room with 100 class plastic bag
4.	Diamond on Oxide Wafer, 10x10mm, 2um Thick, 10nm Ra	<u>Specifications:</u> <ul style="list-style-type: none"> • Wafer Size: 10x10mm • Si wafer Orientation: (100) +/- 0.5o • Insulating Layer: SiO₂ • Diamond film thickness: 2 microns, Oxide Layer: 1 micron • Resistivity: 10E3 ~ 10E4 ohm-cm • Surface Roughness: as grown , RA < 10 nm • Package: One 1000 class clean room with 100 class plastic bag
5.	Diamond on Silicon Wafer, 10x10mm , 2 um Thick, 10	<u>Specifications:</u> <ul style="list-style-type: none"> • Wafer Size: 10x10

	nm Ra	<ul style="list-style-type: none"> • Silicon wafer Orientation: (100) + / - 0.5o • Diamond film thickness: 2 micron • Resistivity: 10E3 ~ 10E4 ohm-cm • Surface roughness: one sides CMP polished with surface roughness < 10 A • Package: One 1000 class clean room with 100 class plastic bag
6.	Electric Conductive Diamond on Insulator Wafer, 10x10 , 2 um Thick, 10 nm Ra	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Wafer Size: 10x10mm • Si wafer Orientation: (100) + / - 0.5o • Insulating Layer: SiO2 • Diamond film thickness: 2 micron, Oxide Layer: 1 micron • Resistivity: <0.1 ohm-cm • Surface Roughness: as grown , RA < 10 nm • Package: One 1000 class clean room with 100 class plastic bag
7.	Diamond on Silicon Wafer, 4" , 1 um Thick, 1nm Ra	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Wafer Size: 4" diameter x 0.5mm • Silicon wafer Orientation: (100) + / - 0.5o • Diamond film thickness: 1 micron • Resitivity: 103 ~ 104 Ohm-cm • Surface roughness: one sides CMP polished with surface roughness < 10 A • Package: One 1000 class clean room with 100 class plastic bag
8.	Diamond on Silicon Wafer, 10x10mm, 0.1 micron Thick, Ra<1 nm	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Wafer Size: 10x10mm • Si wafer Orientation: (100) Prime grade,P-type , B-doped • Diamond film: 100 nm Aqua25 • Diamond film thickness: 01 micron, • Diamond Resistivity: 1000-10000 ohm-cm • Surface Roughness: as grown , RA < 1 nm • Package: One 1000 class clean room with 100 class plastic bag

9. GaN Template on Sapphire & Silicon

A. GaN Template on Sapphire

No.	Item	Description
1.	Mg-doped GaN (0001) Epitaxial Template on Sapphire P type, 2"x 3 micron, 1sp	<p>Mg- doped GaN (0001) Epitaxial Template on sapphire is made by MOCVD -based method.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Mg- doped GaN Epitaxial Template on sapphire • Sizes 2" Round • GaN (0001) thin film layer thickness 3 microns • Dimensions 50.8mm +/- 0.25mm • Conduction Type: P-type, • Resistivity 3.0~5.0 Ohm-cm • Carrier Concentration: (1E17-3E18)/cc • Hole Mobility: 20 cm²/V • FWHM of Rocking Curve for (00.2) reflection for 2 um and 3 um is around 350 arcsec • FWHM of Rocking Curve for (10.2) reflection for 2 um and 3 um is around 450 arcsec • The condition of front surface of the template is "as grown" with Ga face • Substrate: Sapphire (0001) • Orientation (0001) miscut: 0.2 deg +/- 0.1 deg toward M plane • one side polished with the condition of back surface " as-received finish"

2.	Mg-doped GaN Epitaxial Template on Sapphire Ptype, 2"x 2 micron,1sp	<p>Mg- doped GaN Epitaxial Template on sapphire is made by MOCVD -based method.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Mg- doped GaN Epitaxial Template on sapphire • Sizes 2" Round • GaN (0001) thin film layer thickness 2 microns • Dimensions 50.8mm +/- 0.25mm • Resistivity 2.0~4.0 Ohm-cm • Carrier Concentration: (0.1-3)E18/cc • Hole Mobility: 20 cm²/V • FWHM of Rocking Curve for (00.2) reflection for 2 um and 3 um is around 350 arcsec • FWHM of Rocking Curve for (10.2) reflection for 2 um and 3 um is around 450 arcsec • The condition of front surface of the templates is "as grown" with Ga face • Substrate: Sapphire (0001) • Orientation: (0001) miscut 0.2 deg +/- 0.1 deg toward M plane • One side polished with the condition of back surface is "as received finish".
3.	Si-doped GaN (0001) Epitaxial Template on Sapphire N-type, 2"x 4.5 micron,1sp	<p>Si- doped GaN Epitaxial Template on sapphire is made by MOCVD -based method.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Si- doped GaN Epitaxial Template on sapphire • GaN (0001) thin film layer thickness 4.5 microns • Sizes 2" Round • Dimensions 50.8mm +/- 0.25mm • Conduction Type: N-type, • Resistivity: 2.5E-3 Ohm-cm • Carrier Conc: 1E19 /cc • FWHM of RC for the symmetric (002) reflection : ~ 250 arcsec; • FWHM of RC for the asymmetric (102) reflection : ~350 arcsec • The condition of front surface: is as grown with Ga face • Substrates: sapphire • (0001) miscut: 0.2 deg +/- 0.1 deg toward M plane • Thickness of sapphire: 430 um +/- 15 um • One side polished with the condition of back surface is " as received"

B. GaN Template on Silicon

No.	Item	Description
1.	GaN Epitaxial Template on 2" Silicon Wafer, GaN film, N type, undoped on Si (111) substrates, 2"x 500 nm, 1sp	<p>GaN Epitaxial Template on silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template on silicon is a cost effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Nominal GaN thickness: 0.5μm ± 0.1 μm • Front Surface finish (Ga-face): <1nm RMS, As-grown, Epi-ready • Back surface finish: as received • GaN orientation: C-plane (00.1) • Polarity: Ga-face • Conduction Type: Undoped (N-) • Macro Defect Density: <5/cm² • Wafer base: Silicon [111], N type, P doped, res: 0-10 ohm-cm, 2" diameter x 0.5mm, one side polished
2.	GaN Epitaxial Template on 2" Silicon Wafer, GaN film, N type, undoped on Si	<p>-GaN Epitaxial Template on silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template on silicon is a cost</p>

	(111) substrates, 2"x 500 nm, 2sp	<p>effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Nominal GaN thickness: 0.5μm \pm 0.1 μm Front Surface finish (Ga-face): <1nm RMS, As-grown, Epi-ready Back surface finish: Silicon as received GaN orientation: C-plane (00.1) Polarity: Ga-face Conduction Type: Undoped (N-) Macro Defect Density: <1/cm² Wafer base: Silicon [111], N type, P doped, 0-10 ohm-cm, 2" diameter x 0.5mm, both sides polished
3.	GaN Epitaxial Template on 4" Silicon Wafer, GaN film, 0.5 μ m th, N type, undoped, on Si (111) substrates, 4"x 500 nm, 1sp R: 70-85 ohm.cm	<p>GaN Epitaxial Template on silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template on silicon is a cost effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Nominal GaN thickness: 0.5μm \pm 0.1 μm Front Surface finish (Ga-face): <1nm RMS, As-grown, Epi-ready Back surface finish: Silicon as received GaN orientation: C-plane (00.1) Polarity: Ga-face Conduction Type: Undoped (N-) Resistivity: 70-85 ohm-cm Macro Defect Density: <5/cm² Wafer base: Silicon [111], N type, P doped, Res: 0-10 ohm-cm, 4" diameter x 0.5mm, one side polished
4.	GaN Epitaxial Template on 4" Silicon Wafer, GaN film, 0.5 μ m th, N type, undoped, on Si (111) substrates, 4"x 500 nm, 1sp R:<0.5 ohm.cm	<p>GaN Epitaxial Template on silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template on silicon is a cost effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Nominal GaN thickness: 0.5μm \pm 0.1 μm Front Surface finish (Ga-face): <1nm RMS, As-grown, Epi-ready Back surface finish: as received GaN orientation: C-plane (00.1) Polarity: Ga-face Conduction Type: Undoped (N-) Resistivity: < 0.5 ohm-cm Macro Defect Density: <5/cm² Wafer base: Silicon [111], N-type P-doped R:1-10 ohm.cm; 4" diameter x 0.5mm, one side polished
5.	GaN Epitaxial Template on Silicon Wafer, N type, undoped, 10x10 mm x 500 nm,	<p>GaN Epitaxial Template on silicon is made by a hydride vapor phase epitaxy (HVPE)-based method. During the HVPE process, HCl reacts with molten Ga to form GaCl, which in turn reacts with NH₃ to form GaN. Epi GaN template on silicon is a cost effective way to replace GaN single crystal substrate.</p> <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Nominal GaN thickness: 0.5μm \pm 0.1 μm Front Surface finish (Ga-face): <1nm RMS, As-grown, Epi-ready Back surface finish: Silicon (111) N-type P-doped R:0-10 ohm.cm GaN orientation: C-plane (00.1) Polarity: Ga-face Conduction Type: Undoped (N-) and resistivities: < 0.05 Ohm-cm Macro Defect Density: <1/cm² Wafer base: Silicon [111], 10x10x0.5mm, one side polished

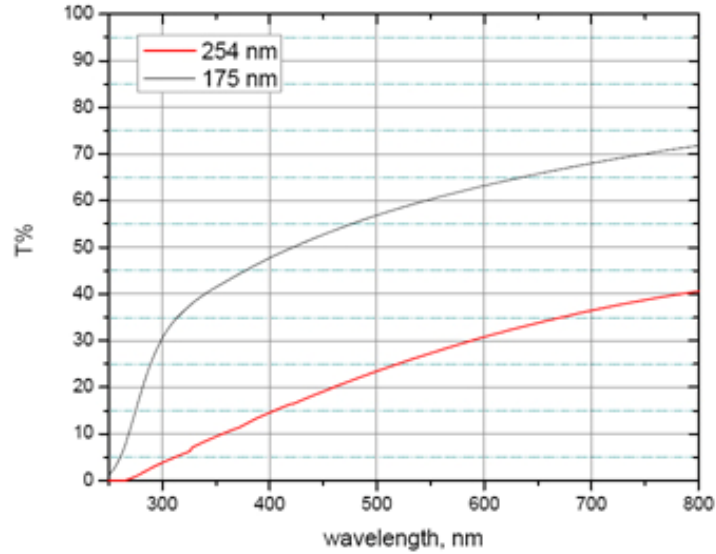
10. Graphene film on Ni/SiO₂/Si

No.	Item	Description
1.	Graphene film on Ni/SiO ₂ /Si 100mm dia,	<p>Graphene™ films are grown directly on a Ni/SiO₂/Si deposited on an oxidized silicon wafer using a CVD process.</p> <p><u>Specifications:</u> Research Grade , about 90 % useful area</p> <ul style="list-style-type: none"> • Wafer Size: 100 mm diameter • Growth Method: Chemical Vapor Deposition (CVD) Technique • Film thickness: 1-10 monolayer thick <ul style="list-style-type: none"> ▪ Graphene film is multilayer with thickness varying in the range 1-10 layers; ▪ Graphene layers are aligned relative to each (graphite-like A-B stacking) other as indicated by the Raman spectrum ▪ The graphene is grown on Ni film by CVD process. ▪ Nickel film is deposited on the substrate covered by thermally grown oxide layer ▪ Thickness of the Ni layer is 300 nm; ▪ The thickness of the silicon oxide layer is 500 nm; ▪ The thickness of the wafer is 500 um ▪ The crystallographic orientation of silicon is 100; • Films are continuous with low defect density. • Atomically thin carbon film (1-10 layer) • Outstanding electronic properties • Chemical inertness and stability • Unprecedented mechanical strength

11. Graphene Oxide Thin Film on Glass

No.	Item	Description
1.	Graphene Oxide Thin Film on Glass, D=50.8 mm, thickness=1 mm	<p>Graphene oxide films can be prepared on different substrates as well, such as PET, quartz, wafers, or substrates provided by a customer. The transparency and thickness of the GO films can be adjusted according to customer requirements.</p> <p><u>Application: Graphene oxide films:</u></p> <ul style="list-style-type: none"> • Flexible nonvolatile memory • Production of Reduced Graphene Oxide (RGO) films, which can be applied in thin film transistors • Transparent conductors • Gas sensors • Supercapacitors • Electronic and optoelectronic devices <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Diameter of Graphene Oxide Film: 35 mm • Thickness: 175 nm • Deposited on a round slide: D=50.8 mm, thickness=1 mm

Optical transmittance in the visible range.



12. InGaAs EPI on InP(Semi-insulating)

No.	Item	Description																														
1.	2" dia. wafer InGaAs EPI on InP (Semi-insulating)(100) by MOCVD deposition substrate (eg InP:Fe)	<p>2" dia. wafer InGaAs EPI on InP (Semi-insulating)(100) by MOCVD deposition InP Orientation: (100) wafer Size: 2" diameter Resistivity:$>1 \times 10^7$ ohm.cm</p> <p>EPD:$<1 \times 10^4$ /cm² EPI : Lattice matched In/Ga alloy layer of n-typr InGaAs, $N_c > 2 \times 10^{18}$ /cc, Thickness :0.5 um(+/- 20%)</p> <p><i>Typical Properties:</i></p> <table border="1"> <thead> <tr> <th>Dopant</th> <th>Type</th> <th>Carrier Concentration (cm⁻³)</th> <th>Mobility (cm²/V.Sec)</th> <th>Resistivity (ohm-cm)</th> <th>EPD (cm⁻²)</th> </tr> </thead> <tbody> <tr> <td>Undoped</td> <td>N</td> <td>$7.5-9.5 \times 10^{15}$</td> <td>4300-4400</td> <td>$1.6E-1-4.5E-1$</td> <td><5000</td> </tr> <tr> <td>Sn</td> <td>N</td> <td>$0.5 \sim 1.0 \times 10^{18}$ $0.5 \sim 1.0 \times 10^{18}$</td> <td>200 ~ 2400 1500 ~ 2000</td> <td>0.001 ~ 0.002 0.0025~0.007</td> <td>3~5 $\times 10^4$</td> </tr> <tr> <td>Zn</td> <td>P</td> <td>$0.8 \sim 2.0 \times 10^{18}$ $2.5 \sim 4.0 \times 10^{18}$</td> <td>2500 ~ 3500 1300 ~ 1600</td> <td>0.0025 ~ 0.006</td> <td>1~ 3 $\times 10^4$</td> </tr> <tr> <td>Fe</td> <td>Semi-Insulating</td> <td>N/A</td> <td>1550-1640</td> <td>$(2.1-2.7) \times 10^7$</td> <td><5000</td> </tr> </tbody> </table>	Dopant	Type	Carrier Concentration (cm ⁻³)	Mobility (cm ² /V.Sec)	Resistivity (ohm-cm)	EPD (cm ⁻²)	Undoped	N	$7.5-9.5 \times 10^{15}$	4300-4400	$1.6E-1-4.5E-1$	<5000	Sn	N	$0.5 \sim 1.0 \times 10^{18}$ $0.5 \sim 1.0 \times 10^{18}$	200 ~ 2400 1500 ~ 2000	0.001 ~ 0.002 0.0025~0.007	3~5 $\times 10^4$	Zn	P	$0.8 \sim 2.0 \times 10^{18}$ $2.5 \sim 4.0 \times 10^{18}$	2500 ~ 3500 1300 ~ 1600	0.0025 ~ 0.006	1~ 3 $\times 10^4$	Fe	Semi-Insulating	N/A	1550-1640	$(2.1-2.7) \times 10^7$	<5000
Dopant	Type	Carrier Concentration (cm ⁻³)	Mobility (cm ² /V.Sec)	Resistivity (ohm-cm)	EPD (cm ⁻²)																											
Undoped	N	$7.5-9.5 \times 10^{15}$	4300-4400	$1.6E-1-4.5E-1$	<5000																											
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Fe	Semi-Insulating	N/A	1550-1640	$(2.1-2.7) \times 10^7$	<5000																											

13. Si+SiO₂+Pt (Polycrystalline)Thin Film

No.	Item	Description
1.	SiO ₂ +Pt thin film on Si (B-doped)substrate ,10x10x0.5mm,1sp (SiO ₂ =500nm, Pt=60nm)	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: SiO₂+Ti+Pt thin film on Si(B-doped) substrate ,10x10x0.5mm,1sp(SiO₂=500nm,Pt=60nm) Resistivity: <0.005 ohm.cm Size: 10x10 x 0.5 mm Polish: one side polished Surface roughness: < 5A
2.	SiO ₂ +Pt thin film on Si substrate ,4"x0.5mm,1sp P-type B-doped,(SiO ₂ =500nm ,Pt=60nm)	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Film: SiO₂+Pt thin film on Si (P-type) substrate ,4"x0.5mm,1sp <ul style="list-style-type: none"> SiO₂=500nm Pt=60nm Resistivity: <0.005 ohm.cm Substrate Size: 4" diameter +/- 0.5 mm x 0.5 mm thickness Polish: one side polished Surface roughness: < 5A

14. Si+SiO₂+Ti(TiO₂)+Pt (Poly or single crystalline)Thin Film

A. Si+SiO₂ +Ti(or TiO₂)+Pt (111) Highly Oriented Polycrystal

No.	Item	Description
1.	SiO ₂ +Ti+Pt(111) thin film on Si substrate ,4"x0.525mm,1sp P-type B-doped,(SiO ₂ =300nm,Ti=10nm ,Pt(111)=150nm)	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Film: SiO₂+Ti+Pt(111) thin film on Si (P-type) substrate, 4"x0.525mm,1sp <ul style="list-style-type: none"> SiO₂=300nm Ti=10nm Pt(111)=150nm Resistivity: N/A Substrate Size: 4" diameter +/- 0.5 mm x 0.5 mm Polish: one side polished Surface roughness: < 5A
2.	SiO ₂ +TiO ₂ +Pt(111) thin film on Si substrate ,4"x0.525mm,1sp P-type B-doped, (SiO ₂ =300nm,TiO ₂ =20nm ,Pt(111)=150nm)	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Film: SiO₂+TiO₂+Pt(111) thin film on Si (P-type) substrate, 4"x0.525mm,1sp <ul style="list-style-type: none"> SiO₂=300nm TiO₂=20nm Pt(111)=150nm Resistivity: N/A Substrate Size: 4" diameter +/- 0.5 mm x 0.525 mm Polish: one side polished Surface roughness: < 5A

B. Si+SiO₂ +Ti+Pt Polycrystalline

No.	Item	Description
1.	SiO ₂ +Ti+Pt thin film on Si (B-doped)substrate ,10x10x0.5mm,1sp	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: SiO₂+Ti+Pt thin film on Si(B-doped) substrate, 10x10x0.5mm,1sp(SiO₂=500nm,Ti=50nm ,Pt=200nm) Resistivity: <0.005 ohm.cm Size: 10x10 x 0.5 mm Polish: one side polished Surface roughness: < 5A
2.	SiO ₂ +Ti+Pt thin film on Si substrate ,10x5x0.5mm,1sp,B-doped	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: SiO₂+Ti+Pt thin film on Si(B-doped) substrate, 10x5x0.5mm,1sp(SiO₂=500nm,Ti=50nm ,Pt=200nm) Resistivity: <0.005 ohm.cm Size: 10x5 x 0.5 mm Polish: one side polished Surface roughness: < 5A
3.	SiO ₂ +Ti+Pt thin film on Si substrate ,4"x0.5mm,1sp P-type B-doped,(SiO ₂ =500nm,Ti=50nm ,Pt=200nm)	<p><u>Silicon Wafer Specifications:</u></p> <ul style="list-style-type: none"> Film: SiO₂+Ti+Pt thin film on Si (P-type) substrate ,4"x0.5mm,1sp <ul style="list-style-type: none"> SiO₂=500nm Ti=50nm Pt=200nm Resistivity: <0.005 ohm.cm Substrate Size: 4" diameter +/- 0.5 mm x 0.5 mm Polish: one side polished Surface roughness: < 5A

15. SiC Epi Film (3C) on Silicon Wafer

No.	Item	Description
1.	8" SiC-3C Thin Film as grown on Silicon Wafer, 2000nm Thick, 8"Dx0.725t - SiC-3CF-8-20	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> Film: SiC Epi film with 3C structure grown by PECVD <ul style="list-style-type: none"> Thickness: 2,000 nm +/- 5% Orientation: (100) Type and Dopant: N type with unintentional doping Surface: as grown (no CMP) Silicon Wafer: 200mm Dia. x 0.725mm Thickness, <100> Orientation <ul style="list-style-type: none"> Type: N/ P doped Resistivity: 1- 20 ohm.cm Polish: one side polished
2.	8" SiC-3C Thin Film as grown on Silicon Wafer, 300nm Thick, 8"Dx0.725t - SiC-3CF-8-03	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> Film: SiC Epi film with 3C structure grown by PECVD <ul style="list-style-type: none"> Thickness: 300 nm +/- 5% Orientation: (100) Type and Dopant: N type with unintentional doping Surface: as grown (no CMP) Silicon Wafer: 200mm Dia. x 0.725mm Thickness, <100> Orientation <ul style="list-style-type: none"> Type: N/ P doped Resistivity: 1- 20 ohm.cm Polish: one side polished

3.	2"x2" SiC-3C Thin Film as grown on Silicon Wafer, 300nm Thick, - SiC-3CF-2-2-03	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Film: SiC Epi film with 3C structure grown by PECVD <ul style="list-style-type: none"> ▪ Thickness: 300 nm +/- 5% ▪ Orientation: (100) ▪ Type and Dopant: N type with unintentional doping ▪ Surface: as grown (no CMP) • Silicon Wafer: 50 x 50 x 0.725mm Thickness, <100> Orientation <ul style="list-style-type: none"> ▪ Type: N/ P doped ▪ Resistivity: 1- 20 ohm.cm ▪ Polish: one side polished
4.	4" SiC-3C Epi Film as CMP on Silicon Wafer, 3.3 micron Thick, - SiC-3CP-4-03	<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Film: SiC Epi film with 3C structure grown by PECVD <ul style="list-style-type: none"> ▪ Thickness: 3300 nm +/- 10% (can be grown up to 20 micron th; the price would be increased with the requested film thickness) ▪ Orientation: 3C SiC (100) ▪ Surface: CMP (film chemical mechanical polished) ▪ Target doping level: 1.0E17 - 1.0E18 /cc (Available Doping range: 1E16 - 1E19 /cc) ▪ Type and dopant: N type, Nitrogen doping • Silicon substrate: <ul style="list-style-type: none"> ▪ Size: 100 mm dia x 0.525 mm thickness ▪ Orientation: (100) ▪ Type: N type / P doped (P type is available as well) ▪ Resistivity: 1- 10 ohm.cm (resistivity is dependent on the doping level) ▪ Polish: one side polished

16. Silicon Nitride film on Silicon Wafer

No.	Item	Description
1.	Silicon Nitride Film on Silicon Wafer, 100 nm / 4" -- Si3N4-Si-4-100nm	<p><u>Silicon Nitride Film:</u></p> <ul style="list-style-type: none"> • Si3N4 Film coated by PECVD method • Si3N4 Thickness: 100nm +/- 10% • Si3N4 covers both side of Silicon wafer <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: Si n- type • Resistivity: < 0.02 ohm-cm • Size: 4" diameter +/- 0.5 mm x 0.525 +/- 0.025 mm th • Orientation: (100) +/- 0.5o • Polish: One sides polished • Surface roughness: Prime • Packing: Vacuum packed on a 4" single wafer carrier box

17. SiO2 +Si3N4 on Silicon wafer

No.	Item	Description
1.	300 nm SiO2 Layer+ 50nm Si3N4(both sides) on Si (100), 2" dia x 0.250 mm t, P type , B-doped R:<0.01-0.1ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO2(300nm)+50nm Si3N4 layer on 2" Silicon wafer(Both sides) • Oxide layer thickness: 300 nm (2000A) +/-10% • Si3N4 thickness:50nm(Both sides) • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455

		<ul style="list-style-type: none"> Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: Si P type/ Boron doped Resistivity: 0.01-0.1 ohm-cm Size: 50.8 diameter +/- 0.5 mm x 0.250 +/- 0.025 mm Orientation: (100) +/- 0.5o Polish: Both sides polished Surface roughness: < 5A
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18. SOS (silicon on Sapphire)

No.	Item	Description
1.	Silicon-on-Sapphire (11-02, R Plate), 100mm Dia x0.6um thick,1sp	<p>Silicon on sapphire (SOS) is a hetero-epitaxial process for integrated circuit manufacturing that consists of a thin layer (typically thinner than 0.6 micrometres) of silicon grown on a sapphire (Al₂O₃) wafer. SOS is part of the Silicon on Insulator (SOI) family of CMOS technologies. SOS is primarily used in aerospace and military applications because of its inherent resistance to radiation.</p> <p>U.S. Dept. of Commerce requires End User Certificate for exporting this product. Oversea end users must file the end user certificate form (click to download) and all sales are subject to get approval by U.S. Dept. of Commerce before shipping.</p> <p><u>Silicon EPI Layer:</u></p> <ul style="list-style-type: none"> Silicon Orientation: (100) Type, Dopant: Intrinsic type, undoped Silicon Thickness: 0.6um +/- 0.06 um Resistivity: >100 ohm.cm Silicon epi film on C plate sapphire is available upon request <p><u>Sapphire Wafer:</u></p> <ul style="list-style-type: none"> R plane -- (1-102) with single flat Wafer size: 100mm dia x 0.53 mm thickness Orientation Flat Length: 32.5mm +/-2.5mm , Flatness:10um, Parallelism:20um Polished surface: Wafer surface is EPI polished via a special CMP procedure. One side polished Projected C-Axis: 45 degree +/- 2 degree Backside Surface: fine ground and etched; Roughness: Ground-64u" Ra
2.	Silicon-on-Sapphire (11-02, R Plate), 10mmx10mm x0.6um thick,1sp	<p>Silicon on sapphire (SOS) is a hetero-epitaxial process for integrated circuit manufacturing that consists of a thin layer (typically thinner than 0.6 micrometres) of silicon grown on a sapphire (Al₂O₃) wafer. SOS is part of the Silicon on Insulator (SOI) family of CMOS technologies. SOS is primarily used in aerospace and military applications because of its inherent resistance to radiation.</p> <p><u>Silicon EPI Layer:</u></p> <ul style="list-style-type: none"> Silicon Orientation: (100) Type, Dopant: Intrinsic type, undoped Silicon Thickness: 0.6um +/- 0.06 um Resistivity: >100 ohm.cm Silicon epi film on C plate sapphire is available upon request <p><u>Sapphire Wafer:</u></p> <ul style="list-style-type: none"> R plane -- (1-102) with single flat

	<ul style="list-style-type: none"> • Wafer size: 10mmx10mm x 0.6 mm thickness • Polished surface: Wafer surface is EPI polished via a special CMP procedure. • One side polished
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19. Thermal Oxide Wafer

A. Thermal Oxide Wafer 2" Dia.

No.	Item	Description
1.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 2" dia x 0.50 mm t, P type, 1 side polished, R: <0.005 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade, about 80% useful area • SiO₂ layer on 2" Silicon wafer • Oxide layer thickness: 300 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P type/ Boron doped • Resistivity: <0.005 ohm-cm • Size: 50.8 diameter +/- 0.5 mm x 0.50 +/- 0.025 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
2.	Thermal Oxide Wafer: 100 nm SiO ₂ Layer on Si (100), 2" dia x 0.50 mm t, N- type, 1 side polished	<p><u>Thermal oxide wafer Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade, about 80% useful area • SiO₂ layer on 2" Silicon wafer • Oxide layer thickness: 100 nm (1000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N- type/ P- doped • Resistivity: <0.01 ohm-cm • Size: 50.8 +/- 0.5 mm in diameter x 0.5 +/- 0.05 mm th • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
3.	Thermal Oxide Wafer: 50 nm SiO ₂ Layer on Si (100), 2" dia x 0.30 mm t, N type, undoped	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade, about 80% useful area • SiO₂ layer on 2" Silicon wafer • Oxide layer thickness: 50 nm (500A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm

		<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N- type/ Un- doped • Resistivity: >1000 ohm-cm • Size: 50.8 diameter +/- 0.5 mm x 0.3 +/- 0.025 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
4.	Thermal Oxide Wafer: 50 nm SiO2 Layer on Si (100), 2" dia x 0.40 mm t, N- type , 1 side polished	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO2 layer on 2" Silicon wafer • Oxide layer thickness: 50 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N- type/ P- doped • Resistivity: 1 - 10 ohm-cm • Size: 50.8 diameter +/- 0.5 mm x 0.4 +/- 0.025 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
5.	Thermal Oxide Wafer: 50 nm SiO2 Layer on Si (100), 2" dia x 0.40 mm t, P type , 1 side polished	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO2 layer on 2" Silicon wafer • Oxide layer thickness: 50 nm (500A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P type/ Boron doped • Resistivity: 1 - 10 ohm-cm • Size: 50.8 diameter +/- 0.5 mm x 0.4 +/- 0.025 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A

B. Thermal Oxide Wafer 3" Dia.

No.	Item	Description
1.	Thermal Oxide Wafer: 300 nm SiO2 Layer on Si (100), 3" dia x 0.50 mm t, undoped N type, 1SP R:>1000 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO2 layer on 3" Silicon wafer • Oxide layer thickness: 300 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm

		<p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ un-doped • Resistivity: >1000 ohm.cm • Size: 3" diameter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
2.	Thermal Oxide Wafer: 100 nm SiO ₂ Layer on the FRONT SIDE (only) of Si (111), 3" dia x 0.50 mm t, P-type, 1SP	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade, about 80 % useful area • SiO₂ layer on the FRONT SIDE (only) of 3" Silicon wafer • Oxide layer thickness: 100 nm (1000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P-type/ B-doped • Resistivity: 0.1-1.0 ohm.cm • Size: 3" +/- 0.5 mm in diameter x 0.5 mm +/- 0.05 mm th • Orientation: (111) +/- 1o • Polish: one side polished • Surface roughness: < 5A
3.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 3" dia x 0.50 mm t, N-type, P-doped 1SP R:1-10 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade, about 80 % useful area • SiO₂ layer on 3" Silicon wafer • Oxide layer thickness: 300 nm (1000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ P-doped • Resistivity: 1-10 ohm.cm • Size: 3" +/- 0.5 mm in diameter x 0.5 mm +/- 0.05 mm th • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
4.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 3" dia x 0.50 mm t, P-type, B-doped 1SP R:1-10 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade, about 80 % useful area • SiO₂ layer on 3" Silicon wafer • Oxide layer thickness: 300 nm (1000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P-type/ B-doped • Resistivity: 1-10 ohm.cm • Size: 3" +/- 0.5 mm in diameter x 0.5 mm +/- 0.05 mm th • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A

<p>5.</p>	<p>Thermal Oxide Wafer: 300 nm SiO₂ Layer on Si (111), 3" dia x 0.50 mm t, N-type ,P-doped 1SP R:5-15 ohm.cm</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 3" Silicon wafer • Oxide layer thickness: 300 nm (1000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ P-dped • Resistivity: 5-15 ohm.cm • Size: 3" +/- 0.5 mm in diameter x 0.5 mm +/- 0.05 mm th • Orientation: (111) +/- 1o • Polish: one side polished • Surface roughness: < 5A
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C. Thermal Oxide Wafer 4" Dia.

No.	Item	Description
<p>1.</p>	<p>Thermal Oxide Wafer: 50 nm SiO₂ Layer on Si (100), 4" dia x 0.5 mm t, N type , undoped,R:>1000ohm.cm</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 2" Silicon wafer • Oxide layer thickness: 50 nm (500A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N- type/ Un- doped • Resistivity: >1000 ohm-cm • Size: 101mm diameter +/- 0.5 mm x 0.5 +/- 0.025 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
<p>2.</p>	<p>Thermal Oxide Wafer: 100 nm SiO₂ Layer on Si (100), 4" dia x 0.50 mm t, Ntype , 1SP R: < 0.01 ohm.cm</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 100 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ P-dped • Resistivity: < 0.01 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
<p>3.</p>	<p>Thermal Oxide Wafer: 100 nm SiO₂ Layer on Si (100),</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area

	<p>4" dia x 0.50 mm t, Ntype , 1SP R: 0.3-0.6 ohm.cm</p>	<ul style="list-style-type: none"> • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 100 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ P-dped • Resistivity: 0.3-0.6 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
<p>4.</p>	<p>Thermal Oxide Wafer: 100 nm SiO₂ Layer on Si (100), 4" dia x 0.50 mm t, Ntype , 1SP R: 1-10 ohm.cm</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 100 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ P-dped • Resistivity: 1-10 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
<p>5.</p>	<p>Thermal Oxide Wafer: 100 nm SiO₂ Layer on Si (100), 4" dia x 0.50 mm t, Ntype ,As-doped 1SP</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 100 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ As-dped • Resistivity: < 0.005 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
<p>6.</p>	<p>Thermal Oxide Wafer: 100 nm SiO₂ Layer on Si (100), 4" dia x 0.50 mm t, P-type ,B-doped 1SP R:1-10 ohm.cm</p>	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 100 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P-type/ B-dped • Resistivity: 1-10 ohm.cm

		<ul style="list-style-type: none"> • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
7.	Thermal Oxide Wafer: 100 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, P-type ,B-doped 1SP R:1-10 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 100 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P-type/ B-dped • Resistivity: 1-10 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
8.	Thermal Oxide Wafer: 1000 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, Ptype , 1SP,R:1-10 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 1000 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: P-type/ B-dped • Resistivity: 1-10 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
9.	Thermal Oxide Wafer: 500 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, N-type , 1sp	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 500 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC • Refractive index - 1.455 • Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> • Conductive type: N-type/ P-dped • Resistivity: 0.01-0.1 ohm.cm • Size: 4"meter +/- 0.5 mm x 0.5 mm • Orientation: (100) +/- 1o • Polish: one side polished • Surface roughness: < 5A
10.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, N type, 1SP R:1-10 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> • Research Grade , about 80 % useful area • SiO₂ layer on 4 Silicon wafer • Oxide layer thickness: 300 nm (2000A) +/-10% • Growth method - Dry oxidizing at 1000oC

		<ul style="list-style-type: none"> Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: N-type/ P-doped Resistivity: 1-10 ohm.cm Size: 4"meter +/- 0.5 mm x 0.5 mm Orientation: (100) +/- 1o Polish: one side polished Surface roughness: < 5A
11.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, P type, 1SP R:0.001-0.005 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> Research Grade , about 80 % useful area SiO₂ layer on 4 Silicon wafer Oxide layer thickness: 300 nm (2000A) +/-10% Growth method - Dry oxidizing at 1000oC Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: P-type/ B-doped Resistivity: R:0.001-0.005 ohm.cm Size: 4"meter +/- 0.5 mm x 0.5 mm Orientation: (100) +/- 1o Polish: one side polished Surface roughness: < 5A
12.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, P type, 1SP R:0.01-0.05 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> Research Grade , about 80 % useful area SiO₂ layer on 4 Silicon wafer Oxide layer thickness: 300 nm (2000A) +/-10% Growth method - Dry oxidizing at 1000oC Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: P-type/ B-doped Resistivity: R:0.01-0.05ohm.cm Size: 4"meter +/- 0.5 mm x 0.5 mm Orientation: (100) +/- 1o Polish: one side polished Surface roughness: < 5A
13.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, undoped N type, 1SP R:>5000 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> Research Grade , about 80 % useful area SiO₂ layer on 4 Silicon wafer Oxide layer thickness: 300 nm (2000A) +/-10% Growth method - Dry oxidizing at 1000oC Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: N-type/ un-doped Resistivity: >5000 ohm.cm Size: 4"meter +/- 0.5 mm x 0.5 mm Orientation: (100) +/- 1o

		<ul style="list-style-type: none"> Polish: one side polished Surface roughness: < 5A
14.	Thermal Oxide Wafer: 300 nm SiO ₂ Layer on Si (100), 4"dia x 0.525 mm t, N type, 2SP R:1-20 ohm.cm	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> SiO₂ layer on 4 Silicon wafer Oxide layer thickness: 300 nm (2000A) +/-10% Growth method - Dry oxidizing at 1000oC Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: N-type/ P-dped Resistivity: 1-20 ohm.cm Size: 4"meter +/- 0.5 mm x 0.525 mm Orientation: (100) +/- 1o Polish: Two sides polished Surface roughness: < 5A
15.	Thermal Oxide Wafer: 90 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, P type, 1SP	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> Research Grade , about 80 % useful area 90nm SiO₂ layer on 4 " Silicon wafer Oxide layer thickness: 90 nm (2000A) +/-10% Growth method - Dry oxidizing at 1000oC Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: P-ype/ B-dped Resistivity: 0.1-1.0ohm.cm Size: 4"meter +/- 0.5 mm x 0.5 mm Orientation: (100) +/- 1o Polish: one side polished Surface roughness: < 5A
16.	Thermal Oxide Wafer: 1000 nm SiO ₂ Layer on Si (100), 4"dia x 0.50 mm t, N-type , 1sp	<p><u>Thermal oxide Layer:</u></p> <ul style="list-style-type: none"> Research Grade , about 80 % useful area SiO₂ layer on 4 Silicon wafer Oxide layer thickness: 1000 nm (2000A) +/-10% Growth method - Dry oxidizing at 1000oC Refractive index - 1.455 Note: customized oxide layer available upon request from 50 nm - 1000 nm <p><u>Specifications:</u></p> <ul style="list-style-type: none"> Conductive type: N-ype/ P-dped Resistivity: 0.01-0.05-ohm.cm Size: 4"meter +/- 0.5 mm x 0.5 mm Orientation: (100) +/- 1o Polish: one side polished Surface roughness: < 5A

20. YBCO Epi Film on SrTiO₃ , LaAlO₃ or Al₂O₃,LSAT

No.	Item	Description																																									
1.	One Side 100nm YBCO Film on Nb:SrTiO ₃ (wt.0.7%) 10x10x0.5 mm substrate	<p><u>Epitaxial YBCO HTS Thin Film on SrTiO₃ substrate up to 30 mm:</u></p> <p>High T_c superconducting epitaxial thin film commercially available at an affordable price. High quality double side epitaxial thin film up to 3" diameter on LaAlO₃, LSAT, Al₂O₃ and SrTiO₃ single crystal substrate by a unique technology.</p> <p>This will make YBCO thin film available at low cost. Researchers don't need to grow thin film any more, but concentrate their talent on HTSC film related devices, such as microwave filter for wireless and HTSC Squid.</p> <p><u>Specifications:</u></p> <table border="1"> <tr> <td>Epitaxial thin Film Composition</td> <td colspan="2"><100> YBCO</td> </tr> <tr> <td>Film dimension</td> <td>YBCO / LaAlO₃</td> <td>10x10 mm ~ 3" dia.</td> </tr> <tr> <td rowspan="3">both for one side or double side film</td> <td>YBCO / LSAT</td> <td>10x10 mm ~ 2" dia.</td> </tr> <tr> <td>YBCO / Al₂O₃</td> <td>10x10 mm ~3" dia</td> </tr> <tr> <td>YBCO / STO</td> <td>10x10 mm ~ 1" dia.</td> </tr> <tr> <td>Epitaxial FWHM</td> <td colspan="2">< 0.2 o</td> </tr> <tr> <td>Critical Transition Temperature T_c</td> <td colspan="2">> 90 K</td> </tr> <tr> <td>Transition Temp. range ΔT_c</td> <td colspan="2">< 0.5 K</td> </tr> <tr> <td>Critical Current J_c</td> <td colspan="2">2~3 MA/cm² @ 77K 0T</td> </tr> <tr> <td>Surface Resistivity R_s</td> <td colspan="2">< 1 m Ohm @ 10 GHz, 77K, 0T</td> </tr> <tr> <td>Thin film thickness</td> <td colspan="2">200 - 500 nm upon request ,</td> </tr> <tr> <td rowspan="3">Uniformity for 2" wafer</td> <td>Thickness</td> <td>400 nm +/- 10 %</td> </tr> <tr> <td>T_c</td> <td>90K +/- 1 o</td> </tr> <tr> <td>J_c</td> <td>3 +/-0.5 MA/cm² @ 80% wafer center.</td> </tr> <tr> <td>Package</td> <td colspan="2">Sealed in Vacuum in a plastic box and bag.</td> </tr> </table>	Epitaxial thin Film Composition	<100> YBCO		Film dimension	YBCO / LaAlO ₃	10x10 mm ~ 3" dia.	both for one side or double side film	YBCO / LSAT	10x10 mm ~ 2" dia.	YBCO / Al ₂ O ₃	10x10 mm ~3" dia	YBCO / STO	10x10 mm ~ 1" dia.	Epitaxial FWHM	< 0.2 o		Critical Transition Temperature T _c	> 90 K		Transition Temp. range ΔT _c	< 0.5 K		Critical Current J _c	2~3 MA/cm ² @ 77K 0T		Surface Resistivity R _s	< 1 m Ohm @ 10 GHz, 77K, 0T		Thin film thickness	200 - 500 nm upon request ,		Uniformity for 2" wafer	Thickness	400 nm +/- 10 %	T _c	90K +/- 1 o	J _c	3 +/-0.5 MA/cm ² @ 80% wafer center.	Package	Sealed in Vacuum in a plastic box and bag.	
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2.	One Side 100nm YBCO Film on SrTiO ₃ (100) 10x10x0.5 mm substrate	<p><u>Epitaxial YBCO HTS Thin Film on SrTiO₃ substrate up to 30 mm:</u></p> <p>High T_c superconducting epitaxial thin film commercially available at an affordable price. High quality double side epitaxial thin film up to 3" diameter on LaAlO₃, LSAT, Al₂O₃ and SrTiO₃ single crystal substrate by a unique technology.</p> <p>This will make YBCO thin film available at low cost. Researchers don't need to grow thin film any more, but concentrate their talent on HTSC film related devices, such as microwave filter for wireless and HTSC Squid.</p> <p><u>Specifications:</u></p> <table border="1"> <tr> <td>Epitaxial thin Film Composition</td> <td colspan="2"><100> YBCO</td> </tr> <tr> <td>Film dimension</td> <td>YBCO / LaAlO₃</td> <td>10x10 mm ~ 3" dia.</td> </tr> <tr> <td rowspan="3">both for one side or double side film</td> <td>YBCO / LSAT</td> <td>10x10 mm ~ 2" dia.</td> </tr> <tr> <td>YBCO / Al₂O₃</td> <td>10x10 mm ~3" dia</td> </tr> <tr> <td>YBCO / STO</td> <td>10x10 mm ~ 1" dia.</td> </tr> <tr> <td>Epitaxial FWHM</td> <td colspan="2">< 0.2 o</td> </tr> <tr> <td>Critical Transition Temperature T_c</td> <td colspan="2">> 90 K</td> </tr> <tr> <td>Transition Temp. range ΔT_c</td> <td colspan="2">< 0.5 K</td> </tr> <tr> <td>Critical Current J_c</td> <td colspan="2">2~3 MA/cm² @ 77K 0T</td> </tr> <tr> <td>Surface Resistivity R_s</td> <td colspan="2">< 1 m Ohm @ 10 GHz, 77K, 0T</td> </tr> <tr> <td>Thin film thickness</td> <td colspan="2">200 - 500 nm upon request ,</td> </tr> <tr> <td rowspan="3">Uniformity for 2" wafer</td> <td>Thickness</td> <td>400 nm +/- 10 %</td> </tr> <tr> <td>T_c</td> <td>90K +/- 1 o</td> </tr> <tr> <td>J_c</td> <td>3 +/-0.5 MA/cm² @ 80% wafer center.</td> </tr> <tr> <td>Package</td> <td colspan="2">Sealed in Vacuum in a plastic box and bag.</td> </tr> </table>	Epitaxial thin Film Composition	<100> YBCO		Film dimension	YBCO / LaAlO ₃	10x10 mm ~ 3" dia.	both for one side or double side film	YBCO / LSAT	10x10 mm ~ 2" dia.	YBCO / Al ₂ O ₃	10x10 mm ~3" dia	YBCO / STO	10x10 mm ~ 1" dia.	Epitaxial FWHM	< 0.2 o		Critical Transition Temperature T _c	> 90 K		Transition Temp. range ΔT _c	< 0.5 K		Critical Current J _c	2~3 MA/cm ² @ 77K 0T		Surface Resistivity R _s	< 1 m Ohm @ 10 GHz, 77K, 0T		Thin film thickness	200 - 500 nm upon request ,		Uniformity for 2" wafer	Thickness	400 nm +/- 10 %	T _c	90K +/- 1 o	J _c	3 +/-0.5 MA/cm ² @ 80% wafer center.	Package	Sealed in Vacuum in a plastic box and bag.	
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		Critical Current Jc	2~3 MA/cm2 @ 77K OT																																				
		Surface Resistivity Rs	< 1 m Ohm @ 10 GHz, 77K, OT																																				
		Thin film thickness	200 ~ 500 nm upon request ,																																				
		Uniformity for 2" wafer	Thickness 400 nm +/- 10 % Tc 90K +/- 1 o Jc 3 +/-0.5 MA/cm2 @ 80% wafer center.																																				
		Package	Sealed in Vacuum in a plastic box and bag.																																				
10.	YBCO Thin Film 500nm (Two sides) on MgO, 2" dia.x0.5 mm,2sp	<p>High Tc superconducting epitaxial thin film commercially available at an affordable price. High quality double side epitaxial thin film up to 3" diameter on LaAlO3, LSAT, Al2O3 and SrTiO3 single crystal substrate by a unique technology.</p> <p>This will make YBCO thin film available at very low cost. Researchers don't need to grow thin film any more, but concentrate their talent on HTSC film related devices, such as microwave filter for wireless and HTSC Squid.</p> <p><u>Specifications:</u></p> <table border="1"> <tr> <td>Epitaxial thin Film Composition</td> <td colspan="2"><100> YBCO</td> </tr> <tr> <td rowspan="4">Film dimension both for one side or double side film</td> <td>YBCO / LaAlO3</td> <td>10x10 mm ~ 3" dia.</td> </tr> <tr> <td>YBCO / LSAT</td> <td>10x10 mm ~ 2" dia.</td> </tr> <tr> <td>YBCO / Al2O3</td> <td>10x10 mm ~ 3" dia.</td> </tr> <tr> <td>YBCO / STO</td> <td>10x10 mm ~ 1" dia.</td> </tr> <tr> <td>Epitaxial FWHM</td> <td colspan="2">< 0.2 o</td> </tr> <tr> <td>Critical Transition Temperature Tc</td> <td colspan="2">> 90 K</td> </tr> <tr> <td>Transition Temp. range ΔTc</td> <td colspan="2">< 0.5 K</td> </tr> <tr> <td>Critical Current Jc</td> <td colspan="2">2~3 MA/cm2 @ 77K OT</td> </tr> <tr> <td>Surface Resistivity Rs</td> <td colspan="2">< 1 m Ohm @ 10 GHz, 77K, OT</td> </tr> <tr> <td>Thin film thickness</td> <td colspan="2">200 ~ 500 nm upon request ,</td> </tr> <tr> <td>Uniformity for 2" wafer</td> <td colspan="2">Thickness 400 nm +/- 10 % Tc 90K +/- 1 o Jc 3 +/-0.5 MA/cm2 @ 80% wafer center.</td> </tr> <tr> <td>Package</td> <td colspan="2">Sealed in Vacuum in a plastic box and bag.</td> </tr> </table>		Epitaxial thin Film Composition	<100> YBCO		Film dimension both for one side or double side film	YBCO / LaAlO3	10x10 mm ~ 3" dia.	YBCO / LSAT	10x10 mm ~ 2" dia.	YBCO / Al2O3	10x10 mm ~ 3" dia.	YBCO / STO	10x10 mm ~ 1" dia.	Epitaxial FWHM	< 0.2 o		Critical Transition Temperature Tc	> 90 K		Transition Temp. range ΔTc	< 0.5 K		Critical Current Jc	2~3 MA/cm2 @ 77K OT		Surface Resistivity Rs	< 1 m Ohm @ 10 GHz, 77K, OT		Thin film thickness	200 ~ 500 nm upon request ,		Uniformity for 2" wafer	Thickness 400 nm +/- 10 % Tc 90K +/- 1 o Jc 3 +/-0.5 MA/cm2 @ 80% wafer center.		Package	Sealed in Vacuum in a plastic box and bag.	
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21. ZnO thin film on Sapphire

No.	Item	Description
1.	ZnO Epi Film on Sapphire(0001), 2"x0.5mm, N2 -doped , ZnO: 0.5 um	<p><u>ZnO Epi Template Specifications:</u></p> <ul style="list-style-type: none"> Film: ZnO epi film on Sapphire <0001> N2-doped Film thickness: 500 A (0.5 um) Total Thickness Variation: 5% Resistivity: 10--1000 ohm-cm Epi orientation: <0001> Film quality: < 50 arc seconds by double crystal x-ray diffraction 2"meter +/- 0.5 mm x 0.5 mm , <0001>orn. Polish: one side polished Surface roughness: < 5A

22. SOI Wafer (Silicon On Insulator)

No.	Item	Description																																		
1.	SOI Epitaxial Wafer: 4" , 20um (P/Boron) + 2 um SiO2 + 500um Si (undoped)	<p><u>Specifications:</u></p> <table border="1"> <tr> <td colspan="2">Device Layer</td> </tr> <tr> <td>Diameter:</td> <td>100 +/- .1mm</td> </tr> <tr> <td>Type/Dopant:</td> <td>P/Boron</td> </tr> <tr> <td>Orientation:</td> <td><1-0-0>+/- .5 degree</td> </tr> <tr> <td>Thickness:</td> <td>20 +/- .5 um</td> </tr> <tr> <td>Resistivity:</td> <td><0.01 ohm-cm</td> </tr> <tr> <td>Flatness:</td> <td><2um</td> </tr> <tr> <td>Flats:</td> <td>Semi Std.</td> </tr> <tr> <td>Finish:</td> <td>Polished</td> </tr> <tr> <td colspan="2">Buried Thermal Oxide:</td> </tr> <tr> <td>Thickness:</td> <td>2um +/- 5%</td> </tr> <tr> <td colspan="2">Handle Wafers:</td> </tr> <tr> <td>Type/Dopant</td> <td>undoped</td> </tr> <tr> <td>Orientation</td> <td><1-0-0>+/- .5 degree</td> </tr> <tr> <td>Resistivity:</td> <td>>2,000 ohm-cm / FZ</td> </tr> <tr> <td>Thickness:</td> <td>500 +/- 10 um</td> </tr> <tr> <td>Finish:</td> <td>Polished</td> </tr> </table>	Device Layer		Diameter:	100 +/- .1mm	Type/Dopant:	P/Boron	Orientation:	<1-0-0>+/- .5 degree	Thickness:	20 +/- .5 um	Resistivity:	<0.01 ohm-cm	Flatness:	<2um	Flats:	Semi Std.	Finish:	Polished	Buried Thermal Oxide:		Thickness:	2um +/- 5%	Handle Wafers:		Type/Dopant	undoped	Orientation	<1-0-0>+/- .5 degree	Resistivity:	>2,000 ohm-cm / FZ	Thickness:	500 +/- 10 um	Finish:	Polished
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2.	SOI Epitaxial Wafer: 1"x1", 2.5µm (P-doped) +1.0 SiO2 +625um Si (P-type /Boron doped)	<p><u>Specifications:</u></p> <table border="1"> <tr> <td colspan="2">Device Layer</td> </tr> <tr> <td>Size:</td> <td>1" x 1"</td> </tr> <tr> <td>Type/Dopant:</td> <td>P-doped</td> </tr> <tr> <td>Orientation:</td> <td><1-0-0>+/- .5 degree</td> </tr> <tr> <td>Thickness:</td> <td>2.5±0.5µm</td> </tr> <tr> <td>Resistivity:</td> <td>1-4 ohm-cm</td> </tr> <tr> <td colspan="2">Flatness:</td> </tr> <tr> <td>Flats:</td> <td>Semi</td> </tr> <tr> <td>Finish:</td> <td>Polished</td> </tr> <tr> <td colspan="2">Buried Thermal Oxide:</td> </tr> <tr> <td>Thickness:</td> <td>2um +/- 5%</td> </tr> <tr> <td colspan="2">Handle Wafers:</td> </tr> <tr> <td>Type/Dopant</td> <td>undoped</td> </tr> <tr> <td>Orientation</td> <td><1-0-0>+/- .5 degree</td> </tr> <tr> <td>Resistivity:</td> <td>>2,000 ohm-cm / FZ</td> </tr> <tr> <td>Thickness:</td> <td>500 +/- 10 um</td> </tr> <tr> <td>Finish:</td> <td>Polished</td> </tr> </table>	Device Layer		Size:	1" x 1"	Type/Dopant:	P-doped	Orientation:	<1-0-0>+/- .5 degree	Thickness:	2.5±0.5µm	Resistivity:	1-4 ohm-cm	Flatness:		Flats:	Semi	Finish:	Polished	Buried Thermal Oxide:		Thickness:	2um +/- 5%	Handle Wafers:		Type/Dopant	undoped	Orientation	<1-0-0>+/- .5 degree	Resistivity:	>2,000 ohm-cm / FZ	Thickness:	500 +/- 10 um	Finish:	Polished
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	Resistivity:	>2,000 ohm-cm / FZ
	Thickness:	500 +/- 10 um
	Finish:	Polished

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